CLAIMS

What is claimed is:

1. A back-contacted solar cell, comprising:

a p-type bulk semiconductor substrate, having a front side and a backside;

a front side n^+ diffusion emitter layer located on the front side of the semiconductor substrate;

a n-gridline negative ohmic contact located on the backside of the semiconductor substrate;

a solid n^{++} doped conductive via disposed through the thickness of the semiconductor substrate that electrically connects the front side n+ emitter layer to the negative ohmic contact located on the backside of the semiconductor substrate; and

a p-gridline positive ohmic contact located on the back side of the semiconductor substrate;

wherein the conductive via comprises a recrystallized n^{++} doped trail that has been formed after a surface-deposited solute material has migrated completely through the semiconductor substrate from one side to the other, driven by a gradient-driven migration process; and

wherein the solute material is, or contains, an n^{++} dopant material.

2. The solar cell of claim 1, wherein the gradient-driven migration process comprises a thermomigration process, an electromigration process, or a combination of both.

3. The solar cell of claim 1, wherein the front side n^+ diffusion emitter layer comprises a phosphorus n^+ diffusion layer.

4. The solar cell of claim 1, further comprising a backside n^+ diffusion emitter layer located on the backside of the semiconductor substrate.

5. The solar cell of claim 4, wherein the front side n+ diffusion emitter layer is lightly doped, and the backside n^+ diffusion emitter layer is heavily doped.

6. The solar cell of claim 1, further comprising an anti-reflection coating disposed on the front surface of the semiconductor substrate, covering the front side n+ diffusion emitter layer and the front side of the conductive via.

7. The solar cell of claim 1, wherein the solute material comprises one or more n-type dopant materials selected from the group consisting of phosphorus, arsenic, and antimony.

8. The solar cell of claim 7, wherein the solute material additionally comprises one or more carrier metals selected from the group consisting of platinum, gallium, magnesium, indium, silver, copper, aluminum, tin, and gold.

9. The solar cell of claim 8, wherein the solute material comprises one or more ternary alloys selected from the group consisting of silver-gold-antimony, silver-tin-antimony, and silver-aluminum-antimony.

10. The solar cell of claim 9, wherein the solute material comprises silver with about 10 at.% antimony and about 10 at% aluminum.

11. The solar cell of claim 4, further comprising a passivation layer disposed on the back surface of the semiconductor substrate, and disposed in-between the positive and negative ohmic contacts.

12. The solar cell of claim 1, further comprising an array of closely-spaced, solid n^{++} doped conductive vias made by a gradient-driven migration process.

13. The solar cell of claim 12, wherein the spacing between adjacent conductive vias is from about 1 mm to about 2 mm.

14. The solar cell of claim 12, wherein the diameter of the conductive vias is from about 25 microns to about 150 microns.

15. The solar cell of claim 1, wherein the semiconductor substrate comprises one or more semiconducting materials selected from the group consisting of silicon, germanium, indium

gallium phosphide, gallium arsenide, indium antimonide, copper indium gallium diselenide, cadmium telluride, and zinc sulfide.

16. A process for fabricating a back-contacted semiconductor solar cell, comprising:

a) providing a p-type semiconductor substrate;

b) cleaning and etching the semiconductor substrate;

c) screen-printing a patterned diffusion barrier covering an area where a p-type ohmic contact will be formed;

d) diffusing phosphorus into the front and back surfaces of the semiconductor substrate to form front side and backside n^+ emitter layers;

e) removing the patterned diffusion barrier;

f) depositing a closely-spaced array of droplets comprising a solute material;

g) thermomigrating the solute material droplets in a special designed rapid thermal processor, whereby solid n^{++} doped conductive vias are formed that electrically connect the front side n^+ emitter layer to the backside n^+ emitter layer;

h) screen-printing silver paste for negative-polarity n-type ohmic contacts;

i) screen-printing silver paste for positive-polarity p-type ohmic contacts; and

j) firing the substrate.

17. The process of claim 16, wherein the semiconductor substrate comprises one or more semiconducting materials selected from the group consisting of silicon, germanium, indium gallium phosphide, gallium arsenide, indium antimonide, copper indium gallium diselenide, cadmium telluride, and zinc sulfide.

18. The process of claim 16, wherein the solute material droplets are thermomigrated in step g) from the front side to the backside.

19. The process of claim 16, further comprising, before step f), forming a shallow pit on the front surface of the semiconductor substrate in the location where each droplet of solute material is to be deposited in step f).

20. The process of claim 16, further comprising, in-between step f) and step g), depositing a thin dielectric layer to help stabilize the molten drop, prevent evaporation of the dopant, and facilitate entrance of the molten drop into the substrate.

21. The process of claim 16, wherein thermomigrating in step g) comprises using a bank of plasma arc lamps to heat one side of the semiconductor substrate.

22. The process of claim 16, further comprising after step g) removing the re-emerged solute droplet.

23. The process of claim 16, further comprising after step g) depositing an anti-reflection coating on the front surface of the semiconductor substrate; covering the front side n^+ emitter layer and the conductive vias.

24. The process of claim 23, wherein depositing the anti-reflection coating comprises depositing silicon nitride using PECVD.

25. The process of claim 16, further comprising before steps h) and I), depositing a dielectric passivation layer on the backside of the semiconductor substrate.

26. The process of claim 25, wherein the passivation layer is patterned to not cover the areas where ohmic contacts are going to be applied.

27. The process of claim 25, wherein silver paste used for making ohmic contacts comprises aggressive oxide frit particles that can etch through the passivation layer.

28. The process of claim 16, wherein the solute material droplets are thermomigrated in step g) from the backside to the front side.

29. The process of claim 16, wherein the thermomigrating step g) is performed before the diffusing step d).

30. The process of claim 16, wherein the thermomigrating step g) is performed after the diffusing step d).

31. A process for fabricating a back-contacted silicon solar cell, comprising:

a) providing a p-type silicon substrate;

b) cleaning and etching the silicon substrate;

d) diffusing phosphorus into the front and back surfaces of the silicon substrate to form front side and backside n^+ emitter layers;

e) screen-printing resist on the back surface, except where the area where the p-type ohmic contact will be made;

f) drying the resist;

g) removing a portion of the backside n^+ emitter layer that was not covered by the resist;

h) removing the resist layer;

i) depositing a closely-spaced array of droplets comprising a solute material;

j) thermomigrating the solute material droplets in a special designed rapid thermal processor, whereby solid n^{++} doped conductive vias are formed that electrically connect the front side and backside n^+ emitter layers;

k) screen-printing silver paste for negative-polarity n-type ohmic contacts;

l) screen-printing silver paste for positive-polarity p-type ohmic contacts; and

m) firing the substrate.